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(L18 AND MEMOR\$4 NEAR5 (RATE\$1 OR SPEED\$1 OR CLOCK\$1)).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	42

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<u>L19</u>	L18 and memor\$4 near5 (rate\$1 or speed\$1 or clock\$1)	42	<u>L19</u>
<u>L18</u>	15 near25 (bridge\$3 or gate\$1 or crossbar\$1)	222	<u>L18</u>
<u>L17</u>	(request\$ or access\$5 or read\$3 or writ\$5) near5 memor\$4 near5 (rate\$1 or speed\$1 or clock\$1) and l9	83	<u>L17</u>
<u>L16</u>	(request\$ or access\$5 or read\$3 or writ\$5) near5 memor\$4 near5 (rate\$1 or speed\$1 or clock\$1) and l8	94	<u>L16</u>
<u>L15</u>	(request\$ or access\$5 or read\$3 or writ\$5) near5 memor\$4 near5 (rate\$1 or speed\$1 or clock\$1) and l7	1461	<u>L15</u>
<u>L14</u>	15 and l8	0	<u>L14</u>
<u>L13</u>	15 and l7	41	<u>L13</u>
<u>L12</u>	16 and l9	0	<u>L12</u>
<u>L11</u>	16 and l8	0	<u>L11</u>
<u>L10</u>	16 and l7	4	<u>L10</u>

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<u>L9</u>	(710/310,312)![CCLS]	511	<u>L9</u>
<u>L8</u>	(712/43,225)[CCLS]	694	<u>L8</u>
<u>L7</u>	(712/2-300)[CCLS]	10914	<u>L7</u>

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<u>L6</u>	L5 and (request\$ or access\$5 or read\$3 or writ\$5) near5 memor\$4 near5 (rate\$1 or speed\$1 or clock\$1)	53	<u>L6</u>
<u>L5</u>	north near25 south near25 (substrate\$1 or chip)	526	<u>L5</u>
<u>L4</u>	l2 and L3	32	<u>L4</u>
<u>L3</u>	address\$4 near5 space near25 (state\$1 or condition\$1) near4 (machine or process\$3)	521	<u>L3</u>
<u>L2</u>	L1 and (plur\$8 or multipl\$5 or two or second) near8 (state\$1)	2616	<u>L2</u>
<u>L1</u>	debug\$7 near 25 context\$1 nearl5 (id\$1 or identif\$8)	13612	<u>L1</u>

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IEEE JNL IEEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEEE CNF IEEE Conference Proceeding

IEEE STD IEEE Standard

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